REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-9, 13-16 and 20-27 are present in this application, claims 18 and 19 being canceled by way of the present amendment. Claims 3-9 are withdrawn. Amended claims 1, 15 and 27 are supported by Fig. 1. No new matter is believed to be added.

Claims 1, 2, 13-16, 18-25 and 27 are rejected under 35 U.S.C. § 102(b) over U.S. 6,400,471 (Kuo et al.). Claim 26 is rejected under 35 U.S.C. § 103(a) over Kuo et al. in view of US 6,002,446 (Eglit).

The image processing apparatus of claims 1, 15 and 27 includes a buffer memory for image data storage and a compression unit for generated compressed image data. The compressed image data is output directly from the compression unit to a data bus connected to a storage unit and to the compression unit for storing the compressed image data (claims 1 and 15), or a DMA controller controls transfer of the compressed image data between the compression unit and the storage unit, and the compressed image data is output directly from the compression unit, which is connected to the bus, via the bus to the storage unit (claim 27). The compressed image data is not stored in another buffer memory, or transferred through other elements before storing in the storage external to the image processing part, which creates the need for extra processing and increases processing time.

Turning to the § 102(b) rejection, Kuo et al. discloses in Figure 11 an architecture having a line reader 620, DSP 922, JPEG hardware 924 and line writer 650. The architecture is associated with a data structure having a plurality of buffers 1110, 1120, 1130, and 1140. Data is transferred between the buffers in the memory structure and elements 620, 922, 924 and 650. In particular, data is transferred to buffer memory 1140 after being processed in JPEG hardware 924. The data is then sent to line writer 650 which writes data to storage. See column 11, lines 48-54. Kuo et al. also teaches the architecture shown in Figures 13 and

14, where data is sent to buffer 1350 from DMA engine 1430, and then to line writer 650 for writing to storage.

The architecture and data structure taught by Kuo et al. includes numerous steps of storing data in buffers. After processing by JPEG hardware 924 (or DMA engine 1430), the output of JPEG hardware 924 is sent to buffer 1140 and then to line writer 650. Line writer 650 writes data to memory. There is clearly no disclosure or suggestion of the image processing apparatus of claims 1, 15 and 27 where a compression unit and a storage unit are connected to a bus, and a compression unit outputs compressed image data directly to the storage unit via the bus. The storage unit is external to the image processing part. In contrast, buffer 1140 is part of the architecture/stat structure and is not external. The external memory is described as connected to the line writer 650. Kuo et al. teaches the additional storage steps (into buffers 1140 or 1350) and the use line writer 650, which has additional elements increasing the cost and complexity of the architecture/data structure, increases the processing required and processing time. Moreover, there is no bus described connected to both JPEG hardware 924 and the not shown memory connected to line writer 650. The apparatuses of claims 1, 15 and 27 are neither taught nor suggested by Kuo et al.

Eglit is cited for ping-pong buffers. Even if ping-pong buffers are included in the architectures of Kuo et al., the deficiencies noted above in Kuo et al. remain. The apparatuses of claims 1, 15 and 27 are neither taught nor suggested by a combination of Kuo et al. and Eglit.

It is respectfully submitted the present application is in condition for allowance, and a favorable action to that effect is respectfully requested.

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